Abstract

In this work we are going to present a design of a test bed for a superconducting high speed Digital Signal Processor (DSP), designed to run basic matrix-matrix multiplications at a speed of 30 Gops. Main application of the being developed DSP is multi-user detection in a 3G wireless system. The DSP consist of a digital core, RSFQ Multiply Accumulate unit (MAC) and a memory. The memory is divided into two parts: room temperature memory for matrix storing and a fast RSFQ shift register based memory for storing vectors. An RSFQ fast shift-register-memory is located on a Multi Chip Module (MCM) board together with the digital core. Communication between room temperature memory and the cryogenic MCM is performed with an asynchronous protocol at 500 MHz speed for a single channel. To verify the DSP operation a temperature acquisition system receives output data from the DSP at 7M bit/s. The overall structure of the test bed comprises two room temperature blocks for matrix storing and data acquisition controlled by external data source and interface circuitry between semiconductor and superconductor parts. We are going to present results of the heat load calculations, design and specifications of the high speed communication channels, design of the biasing network and of the MCM board.

Symbol level multi-user detection

- Standard DSP fixed point implementation
- Peak performance 30 GMAC per second
- Hybrid semiconductor/superconductor memory - 30 Gword per second memory fetch.

Reduced design and high performance prototype

- Multi-user detector treats all users simultaneously
- multi-user is an add-on component for a standard receiver
- Standard DSP high performance prototype

Fixed point Successive Interference Canceller (SIC)

- DSP consisting of multi-chip module (MCM) with superconducting DSP core and semiconductor memory and interface circuitry.
- 25 Gops can speed and 500 MHz data link speed corresponds to 1 row.
- Limitations
  - Bandwidth, jitter and physical distance of the communication lines connecting memory to the RSFQ based cash memory.
  - 500 MHz per second data transmission and 2 nm jitter between different channels of the bus.

Superconductor DSP components

- 5x2 700 JJs
- 15x5 925 JJs
- 15x15 2033 JJs
- 4 x 4 multiplier free clock 310 JJs
- 5 x 5 multiplier linear clock 450 JJs
- 5-bit serial adder 380 JJs
- High speed test bench 158 JJs
- Hypres 4.5 kA/cm²

Increased circuit complexity with Multi Chip Modules (MCM)

- Limited yield of RSFQ circuit fabrication leads to the necessity of dividing the different circuits into sub-chips.
- Development of an RSFQ DSP requires MCM packaging technique, due to the large chip area required.
- Separate RSFQ sub-chips can be tested and verified individually.

Multi Chip Module cryo probe

- 134 Be-Cu gold plated spring contacts.
- 126 ground pads (for high frequency properties and even current return).

Conclusion

In our work we propose implementation of one simple processor with the record performance of 30 10-bit fixed point 10-multiply-accumulate per second combining ultra high speed of the superconducting RSFQ digital technology and high capacity of the semiconductor memory. The full of the circuit design and testing work is concentrated in the high frequency circuitry of the entire chip with small size. The cryo probe is the most important component. we have fabricated a Hypres 4.5 kA/cm² process. The digital core is the RSFQ Multiply Accumulate unit, MAC. The MAC consists of multipliers, adders, combiners, and combiner. All components are located in a 30 GHz clock cycle. All components with reduced scale have already been designed and tested at laboratory frequency. The prototype DSP will be tested at high speed using the designed MCM cryo probe with the developed high speed test bench. The implementation of the high bandwidth asynchronous data interface between room temperature electronics and the 1.5 K Bi RSFQ cash memory, is planned as a CMOS First In First Out (FIFO) shift register interface. Future work for implementation of a complete SIC prototype requires solution of the following system of problems: Reshaping technology with more than 10 GHz bandwidth and bit error rate less than 10^-10 8-bit implementation of the high bandwidth asynchronous data interface, optimization of the heat load and noise influence between superconducting and semiconductor chips, mounting of the components on cryocooler.